SPECIFICATION
FOR
LCD MODULE

Customer : _____

CustomerP/N _____

Model No. : ESHX039FHP-NH5

Version : V1.5

Date : 2021-01-13

Final Approval by Customer

LCM Machinery OK ☐	Checked By	
LCM Display OK ☐	Checked By	
LCM NG ☐ LCM OK ☐	Approved By	

Confirmed :

DESIGN	CHECK	APPROVAL

1.0 cm (Type 0.39) Active Matrix Color OLED Panel Module

1. Overview/Application

ESHX039FHP-NH5 is a 0.39 inch（1 cm) diagonal, FHD resolution(1920 x1080), active matrix color OLED (Organic Light Emitting Display)panel module based on single crystal silicon backplane . The pixel circuits and driving IC are integrated on the silicon backplane to get the compact size and very low power consumption.

(Potential applications: Virtual Reality application（AR/VR）, Head mounted displays, Near-Eye Displays etc.)

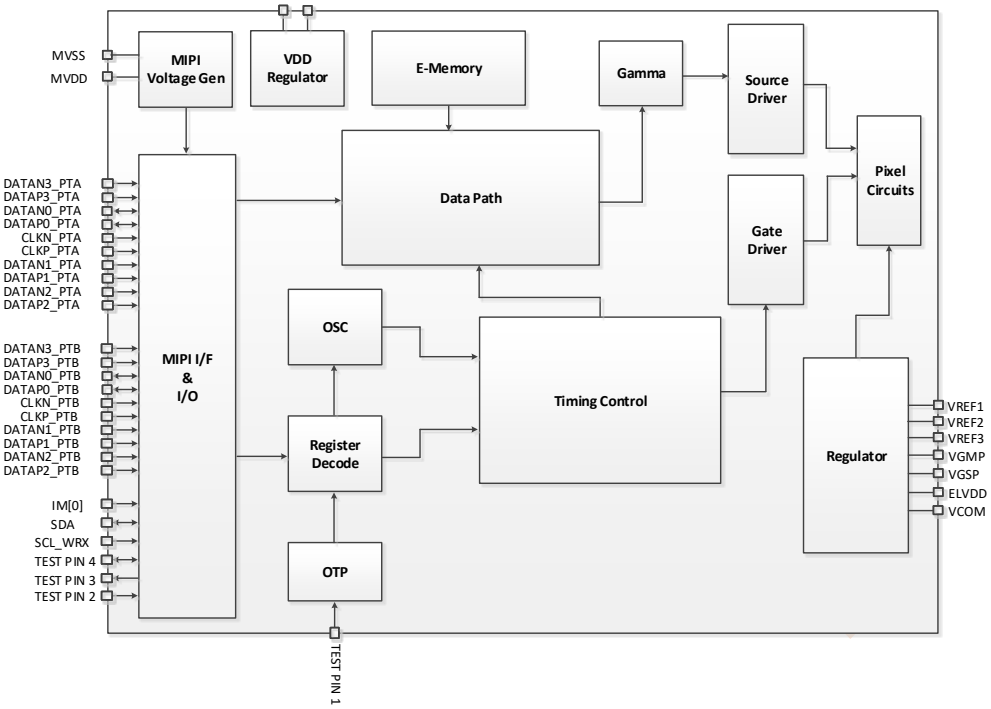
2. Features

- Small-size, high resolution 0.39 FHD Display PPI=5644
- AP Operated Resolution (8*M, M=40~240) x RGB x (8*N, N=30~135)
- Full color mode 16.7M colors
- Fast response
- Thin and light in weight
- Color enhancement, Sharpness enhancement
- High contrast mode
- High fluency mode
- Power-saving (PS) mode
- Scan direction selection, up or down
- Interface, Support MIPI only or MIPI+I^2C

3. Module Structure

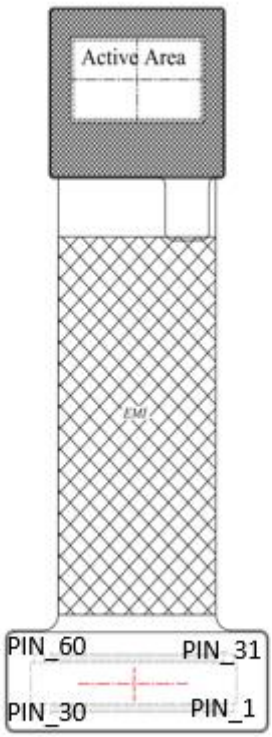
- Active matrix color OLED display with on-chip driver based on single crystal silicon transistors

4. System Block Diagram



5. Pin Description

Pin Assignment



- **FPC module**

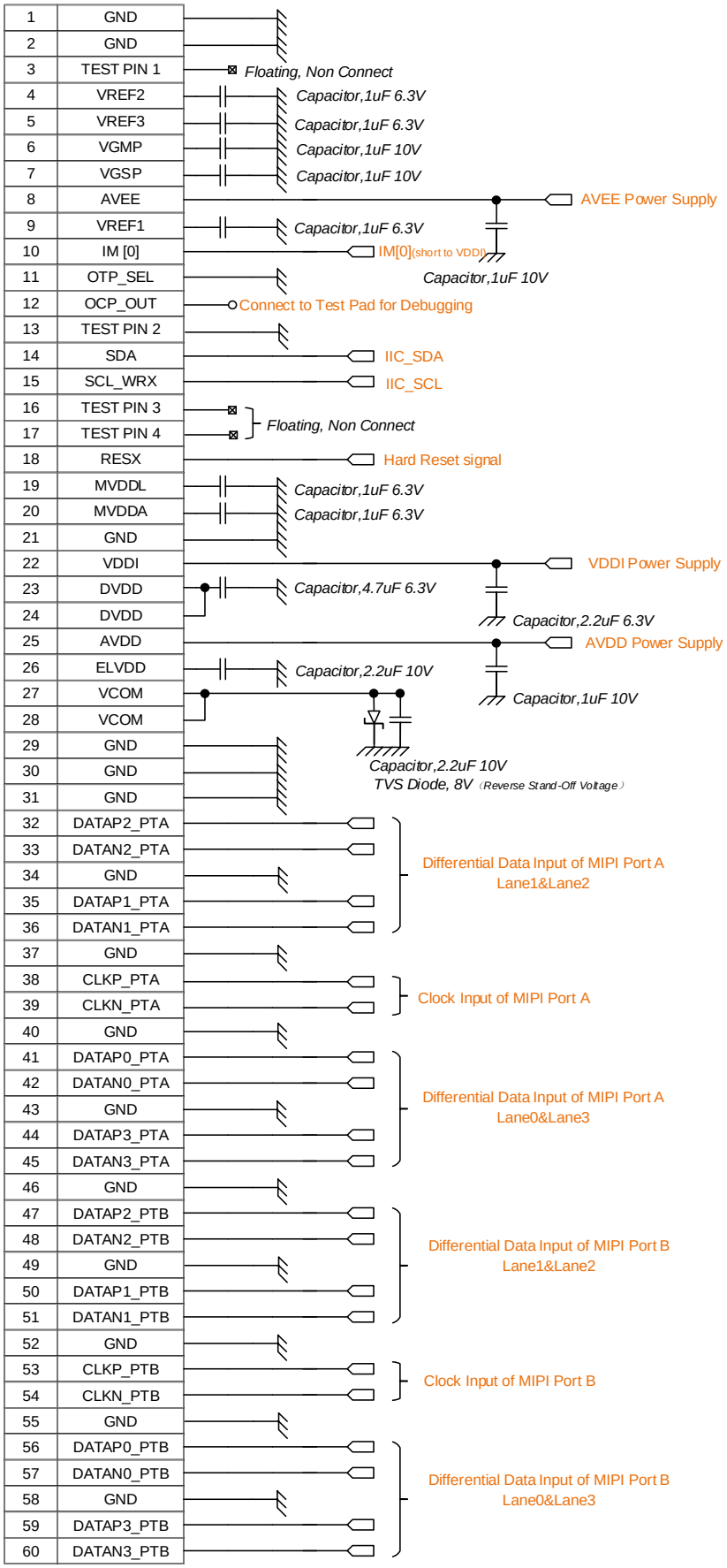
5.1 Pin description

<table>
<tr><th>PIN No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>2</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>3</td><td>TEST PIN 1</td><td>Input</td><td>TEST pin（no connect，Floating)</td></tr>
<tr><td>4</td><td>VREF2</td><td>Output</td><td>VREF voltage，Connect a capacitor for stabilization</td></tr>
<tr><td>5</td><td>VREF3</td><td>Output</td><td>VREF voltage，Connect a capacitor for stabilization</td></tr>
<tr><td>6</td><td>VGMP</td><td>Output</td><td>Gamma top voltage，Connect a capacitor for stabilization</td></tr>
<tr><td>7</td><td>VGSP</td><td>Output</td><td>Gamma bottom voltage，Connect a capacitor for stabilization</td></tr>
<tr><td>8</td><td>AVEE</td><td>Power Supply</td><td>Power supply for OLED cell，Connect a capacitor for stabilization</td></tr>
<tr><td>9</td><td>VREF1</td><td>Output</td><td>VREF voltage，Connect a capacitor for stabilization</td></tr>
<tr><td>10</td><td>IM [0]</td><td>Input</td><td>Use to select the Interface type.
<table>
<tr><th>IM [0]</th><th>Command Execute</th><th>Image Write</th></tr>
<tr><td>0</td><td>MIPI</td><td>MIPI</td></tr>
<tr><td>1</td><td>I2C/MIPI</td><td>MIPI</td></tr>
</table>
Note: Recommend to short to VDDI</td></tr>
<tr><td>11</td><td>OTP_SEL</td><td>Input</td><td>MTP type selection.
OTP_SEL, connect to GND : use internal OTP</td></tr>
<tr><td>12</td><td>OCP_OUT</td><td>Output</td><td>Over current protect flag</td></tr>
<tr><td>13</td><td>TEST PIN 2</td><td>Input</td><td>TEST pin，connect to GND</td></tr>
<tr><td>14</td><td>SDA</td><td>Input/ Output</td><td>Bi-direction data PIN in I2C I/F
If this pin is not used, please connect to VDDI</td></tr>
<tr><td>15</td><td>SCL_WRX</td><td>Input</td><td>Synchronous clock signal in I2C I/F.
If this pin is not used, please connect to VDDI</td></tr>
<tr><td>16</td><td>TEST PIN 3</td><td>Output</td><td>TEST pin，（no connect，Floating)</td></tr>
<tr><td>17</td><td>TEST PIN 4</td><td>Input/ Output</td><td>TEST pin，（no connect，Floating)</td></tr>
<tr><td>18</td><td>RESX</td><td>Input</td><td>This signal will reset the device and must be applied to properly initialize the chip，
Signal is active low</td></tr>
<tr><td>19</td><td>MVDDL</td><td>Output</td><td>Internal system Power，Connect a capacitor for stabilization</td></tr>
<tr><td>20</td><td>MVDDA</td><td>Output</td><td>Internal system Power，Connect a capacitor for stabilization</td></tr>
<tr><td>21</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>22</td><td>VDDI</td><td>Power Supply</td><td>External power supply（1.8V for digital system power）</td></tr>
<tr><td>23</td><td>DVDD</td><td>Output</td><td>Internal system Power，Connect a capacitor for stabilization</td></tr>
<tr><td>24</td><td>DVDD</td><td>Output</td><td>Internal system Power，Connect a capacitor for stabilization</td></tr>
<tr><td>25</td><td>AVDD</td><td>Power Supply</td><td>Power supply for OLED cell，Connect a capacitor for stabilization</td></tr>
</table>

26	ELVDD	Output	Power supply for OLED cell，Connect a capacitor for stabilization
27	VCOM	Output	Power supply for OLED cell，Connect a capacitor for stabilization
28	VCOM	Output	Power supply for OLED cell，Connect a capacitor for stabilization
29	GND	Power Supply	Circuit ground
30	GND	Power Supply	Circuit ground
31	GND	Input	Circuit ground for MIPI
32	DATAP2_PTA	Input	Differential small amplitude signal of MIPI data input
33	DATAN2_PTA	Input	Differential small amplitude signal of MIPI data input
34	GND	Input	Circuit ground for MIPI
35	DATAP1_PTA	Input	Differential small amplitude signal of MIPI data input
36	DATAN1_PTA	Input	Differential small amplitude signal of MIPI data input
37	GND	Input	Circuit ground for MIPI
38	CLKP_PTA	Input	MIPI CLK
39	CLKN_PTA	Input	MIPI CLK
40	GND	Input	Circuit ground for MIPI
41	DATAP0_PTA	Input/ Output	Differential small amplitude signal of MIPI data input
42	DATAN0_PTA	Input/ Output	Differential small amplitude signal of MIPI data input
43	GND	Input	Circuit ground for MIPI
44	DATAP3_PTA	Input	Differential small amplitude signal of MIPI data input
45	DATAN3_PTA	Input	Differential small amplitude signal of MIPI data input
46	GND	Input	Circuit ground for MIPI
47	DATAP2_PTB	Input	Differential small amplitude signal of MIPI data input
48	DATAN2_PTB	Input	Differential small amplitude signal of MIPI data input
49	GND	Input	Circuit ground for MIPI
50	DATAP1_PTB	Input	Differential small amplitude signal of MIPI data input
51	DATAN1_PTB	Input	Differential small amplitude signal of MIPI data input
52	GND	Input	Circuit ground for MIPI
53	CLKP_PTB	Input	MIPI CLK
54	CLKN_PTB	Input	MIPI CLK
55	GND	Input	Circuit ground for MIPI
56	DATAP0_PTB	Input/ Output	Differential small amplitude signal of MIPI data input
57	DATAN0_PTB	Input/ Output	Differential small amplitude signal of MIPI data input
58	GND	Input	Circuit ground for MIPI
59	DATAP3_PTB	Input	Differential small amplitude signal of MIPI data input
60	DATAN3_PTB	Input	Differential small amplitude signal of MIPI data input

5.2 Peripheral Circuit

FPC Module



Mounting the capacitor for each power supply to ensure that the panel display normally.

Notes:

No.	Signal Name	Typical Value	Maximum Rated Voltage	Note
1	VDDI	Cap, 2.2uF	6.3V	
2	AVDD	Cap, 1.0uF	10V	
3	ELVDD	Cap, 2.2uF	10V	
4	AVEE	Cap, 1.0uF	10V	
5	DVDD	Cap, 4.7uF	6.3V	
6	MVDDA	Cap, 1uF	6.3V	
7	MVDDL	Cap, 1uF	6.3V	
8	VGMP	Cap, 1uF	10V	
9	VGSP	Cap, 1uF	10V	
10	VREF1	Cap, 1uF	6.3V	
11	VREF2	Cap, 1uF	6.3V	
12	VREF3	Cap, 1uF	6.3V	
13	VCOM	Cap, 2.2uF TVS	10V	

(1) There are totally 13 capacitors and 1 TVS diode.

(2) The TVS diode is placed between VCOM and ground, and the anode connect to Vcom, the cathode connect to GND.

5.3 Interface

0.39" Micro OLED supports MIPI interface and inter-integrated circuit interface (I2C). 1 port MIPI or 2 port MIPI is selected by register, and I2C is selected by IM0, the detail interface selection by IM0 pin and register of PORT1_2_SEL shows in below table.

IM0	PORT1_2_SEL	Command Execute	Image Write
0	0	MIPI	MIPI 1port
0	1	MIPI	MIPI 2 port
1	0	I2C+ MIPI	MIPI 1port
1	1	I2C+ MIPI	MIPI 2 port

5.3.1 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The master generates all clock pulses, including the acknowledge ninth clock pulse.

5.3.1.1 I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device which should response is addressed first. There are several slave addresses can be selected by MCU. The slave addressing is always

Definition

-Transmitter: The device which sends the data to the bus.

-Receiver: The device which receives the data from the bus.

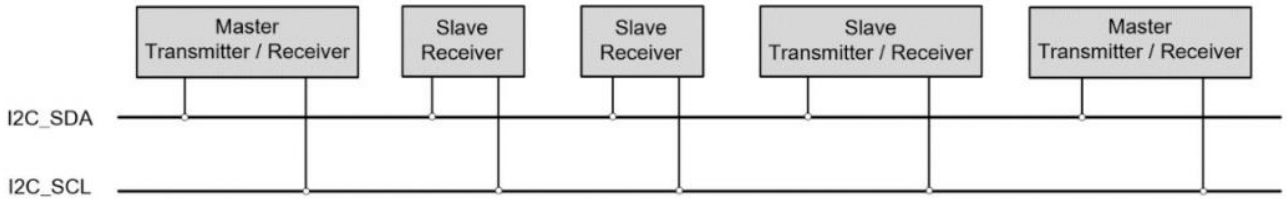
-Master: The device which initiates a transfer, generates clock signals and terminates a transfer.

-Slave: The device addressed by a master.

-Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.

-Arbitration: Procedure to ensure that. If more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

-Synchronization: Procedure to synchronize the clock signals of two or more devices.



5.3.1.2 Write Sequence

0.39" Micro OLED supports register write sequence via I2C-bus transfer. The register writing supports single register write mode. The detailed transfer sequences are illustrated and described as below.

(1) Data transfer for register writing should follow the format shown as below.

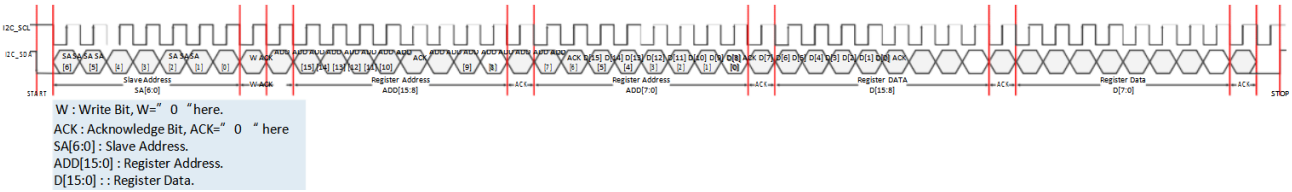
(2)After the START condition, a slave address is sent. R/$\overline{W}$ bit is setting to “0” for Write.

(3)The slave issues an ACK to the master.

(4)8-bits register address transfer first then transfer the register data parameter.

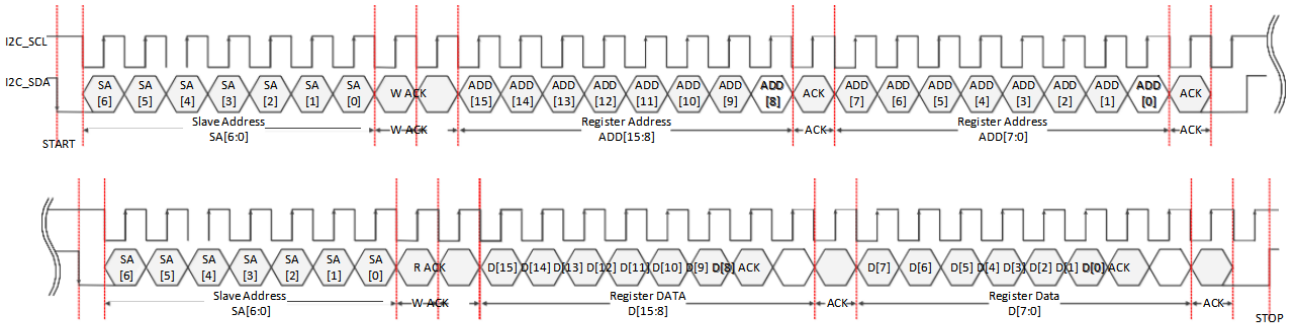
(5)A data transfer is always terminated by a STOP condition.

(6) The chip SA[6:0]=100_1100.



5.3.1.3 Read Sequence

0.39" Micro OLED supports register read sequence via I2C-bus transfer. The register reading supports single register read mode. The register data reading transfer are shown as below.



W : Write Bit, W=" 0 " here.
R : Read Bit, R=" 1 " here.
ACK : Acknowledge Bit, ACK=" 0 " here
SA[6:0] : Slave Address.
ADD[15:0] : Read Register Address.
D[15:0] : : Read Register Return Data.

5.3.2 MIPI Interface

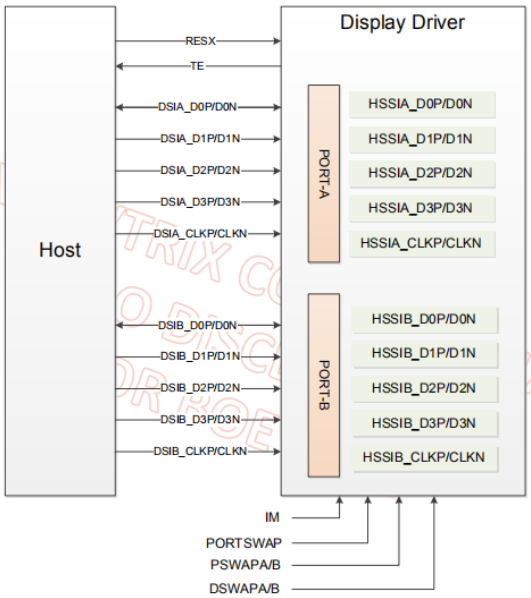
Display serial interface (DSI) specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specification by adoption pixel formats and command set. The detail Lane configuration for DPHY is listed below.

There are one Clock Lane and 1~4 Data Lane. The configuration for DPHY between host and 0.39" Micro OLED shows as the table below.

Lane Pair	Available Operation Mode	
Clock Lane	Unidirectional Lane	Forward High-Speed Clock Escape Mode (ULPS only)
Data Lane 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 3	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

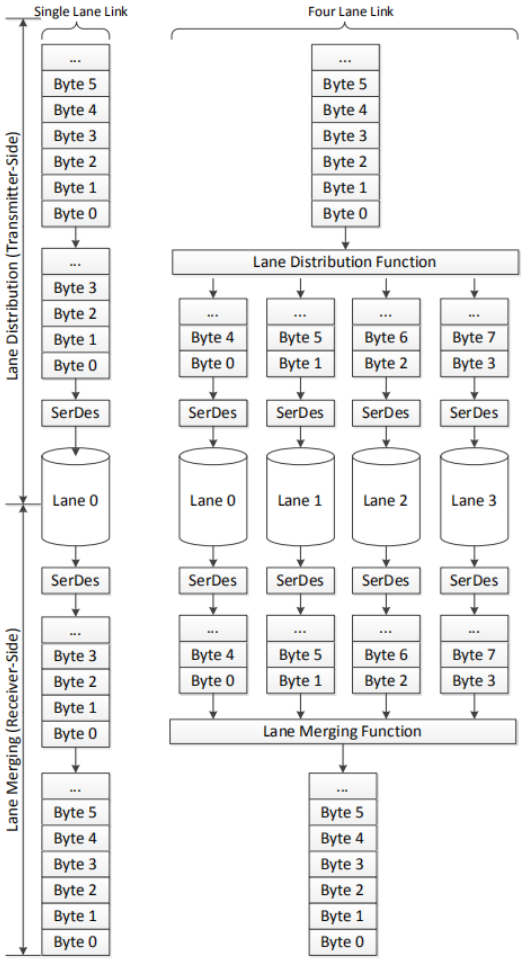
5.3.2.1 DSI System Configuration

0.39" Micro OLED supports MIPI 1 port with 2, 3 or 4 lane configurations for DPHY. The system configuration is shown as the figure below. There are HW pin (IM) and registers (Lane_num_cfg, PSWAP, DSWAP) which can set the interface and lane related configuration



5.3.2.2 Multi-Lane Distribution and Merging

DSI is a lane-scalable interface. Multi-lane implementations shall use a single common clock signal, shared by all data lane. In the transmitter, there will be a layer to distribute a sequence of packet bytes across N Lanes. And in the receiver, there will be a layer to merge this sequence of packet byte back to correct order. The data processing flow is shown as the figure below for DPHY one-lane/four-lane condition.



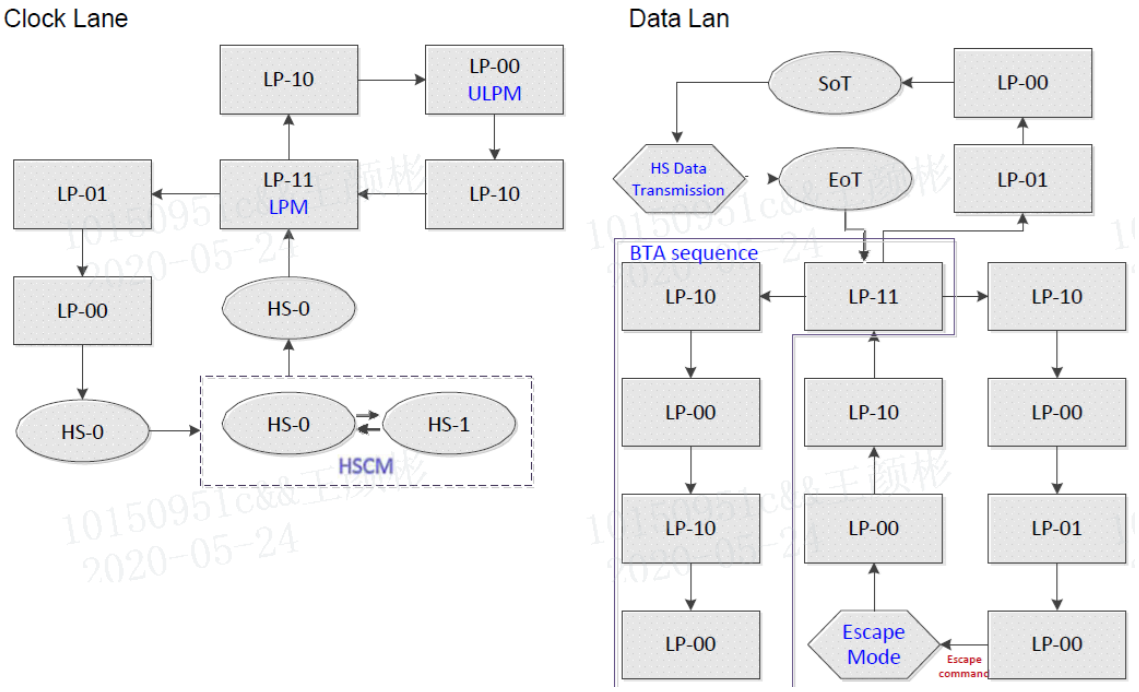
5.3.2.3 Interface Level Communication

DSI uses data and clock lane for DPHY communication. The Lane state is determined by driving certain Line levels. During normal operation, either a HS-TX or a LP-TX is driving a Lane. The HS-TX always drives the Lane differentially. The LP-TX drives two Lines for a Lane independently and single ended. These results of High-Speed Lane states and Low-Power Lane states for DPHY are as the table below.

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

5.3.2.4 Operation Modes

During normal operation a Lane will be either in Control or High-Speed mode. The clock lane can be driven into three different modes: Low-Power Mode (LPM), Ultra-Low-Power Mode (ULPM) or High-Speed Clock Mode (HSCM). The Data Lane can be driven into following different modes: Escape Mode, HS Data Transmission, Bi-directional Data Lane Turnaround (BTA). The entry and leaving protocol flow chart for DPHY are as below.



5.3.2.4.1 Escape Modes

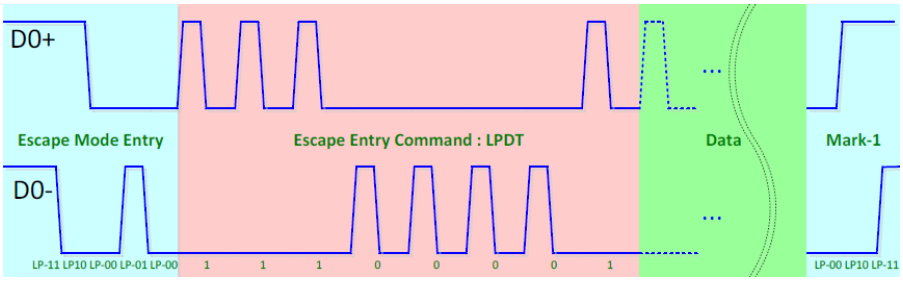
Escape mode is a special mode of operation for Data Lanes using Low-Power stated. With this mode some additional functionality becomes available. A data Lane shall enter Escape mode via Escape mode Entry procedure: LP-11→LP-10→LP-00→LP-01→LP-00. An 8-bit entry command shall be sent to indicate the requested action. The available Escape mode commands and actions are as the table below.

Escape Command	Command Type	Entry Command Pattern (First bit → Last bit)
Low-Power Data Transmission	Mode	1110 0001
Ultra-Low Power State	Mode	0001 1110
Undefined mode	Mode	1001 1111
Undefined mode	Mode	1101 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001
Unknown	Trigger	1010 0000

5.3.2.4.2 Low Power Data Transmission

If the Escape mode Entry procedure is followed up by Entry Command for Low Power Data Transmission (LPDT). Data can be communicated by the protocol at low speed. The LPDT waveform is as follows and the figure below.

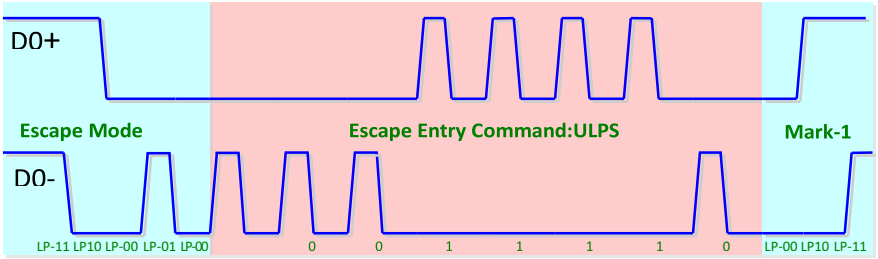
1. Escape mode Entry Sequence
2. Escape Entry Command (87h) for LPDT
3. LP data for LPDT
4. Mark-1 （LP-00→LP-10→LP-11）to leave Escape mode



Ultra-Low-Power State

The MCU can force data lane in Ultra-Low-Power State (ULPS) by Escape Mode with ULPS Entry Command. The sequence to force data lane in ULPS is as follows and the figure below.

1. Escape mode Entry Sequence: LP-11→LP-10→LP-00→LP-01→LP-00.
2. Escape Entry Command (78h) for ULPS
3. Mark-1（LP-00→LP-10→LP-11） to leave Escape mode



5.3.2.5 High-Speed Data Transmission (HSDT)

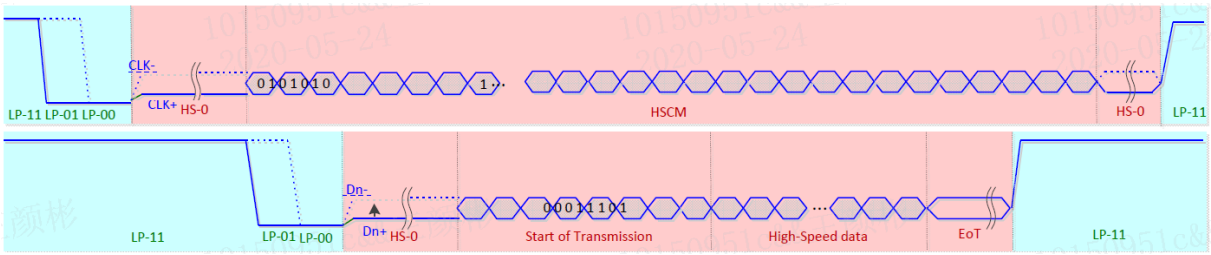
For High-Speed Data Transmission in DPHY, Clock lane have to enter High-Speed Clock Mode (HSCM) before Data lanes enter High-Speed Data Transmission. And the Data lanes have to leave High-Speed Data Transmission after Clock lanes already left HSCM. The High-Speed Data Transmission sequence for DPHY is as the figure below.

■ **Data Lane**

1. HS request sequence: LP-11 → LP-01 → LP-00
2. Keep HS-0 for certain time
3. Start of Transmission sequence (B8h)
4. HS data for HSDT
5. End of Transmission sequence (HS-0 if last data bit is HS-1, HS-1 if last data bit is HS-0)
6. Back to LP-11 to leave HSDT

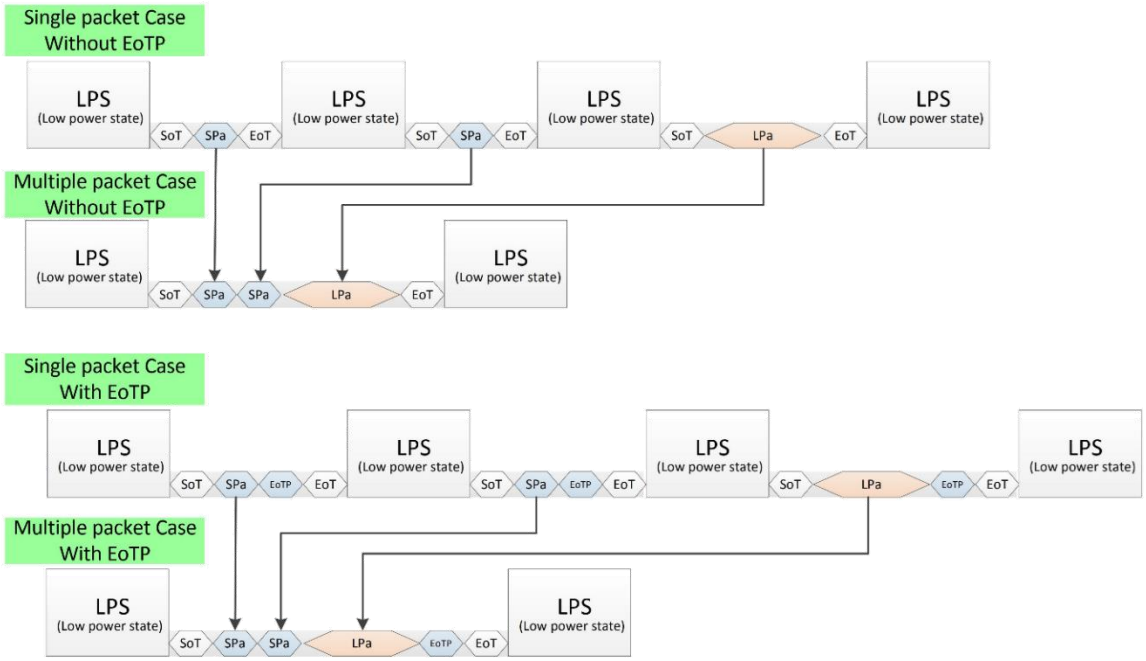
■ **Clock Lane**

1. HS request sequence: LP-11 → LP-01 → LP-00
2. Keep HS-0 for certain time
3. High speed clock mode
4. Keep HS-0 for certain time
5. Back to LP-11 to leave HSCM



5.3.2.6 Burst of High-Speed Data Transmission

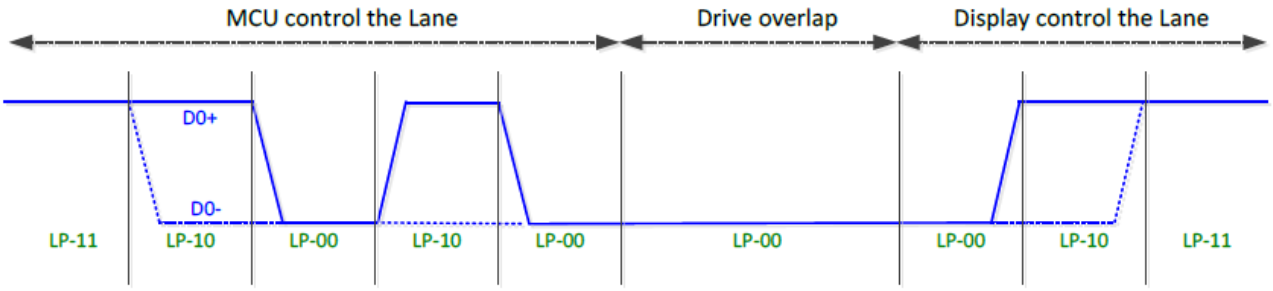
For HSDT, there can be one data packet or multiple packets in one HS burst. These data packets can be long packet (LPa) or Short packet (SPa). HSDT with End of Transmission Packet(EoTP) or without it is selectable. examples are as below.



5.3.2.7 Bi-directional Lane Turnaround (BTA)

The transmission direction of a bi-directional lane can be swapped by means of a turnaround procedure. The procedure enable information transfer in the opposite direction and this procedure is the same for either a change from forward-to-reverse or reverse-to-forward direction. The BTA procedure is as follows and the figure below.

1. MCU send Turnaround Request sequence: LP-11 →LP-10 →LP-00→LP-10 →LP-00
2. MCU change to Hi-Z state and wait for display module start to control the D0 Lane
3. Display module control the Lane and change to stop state: LP-00→LP-10 →LP-11

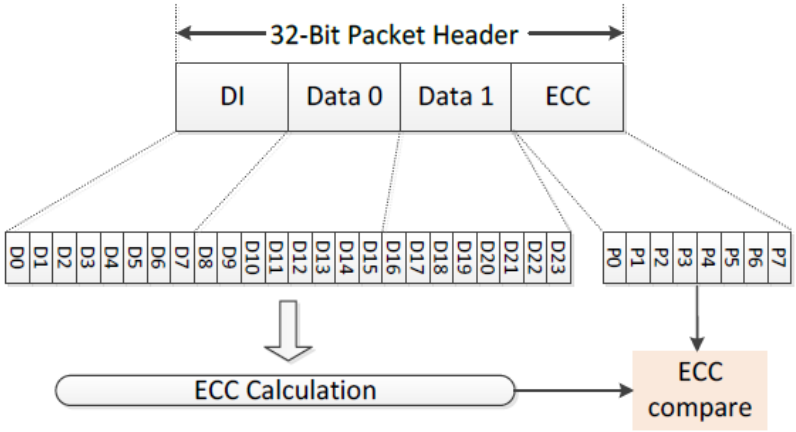


5.3.2.8 Interface Level Communication

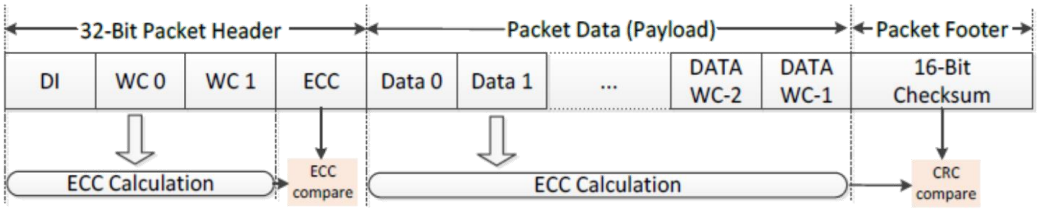
There are two packet structures are defined for communication: Short Packets(SPa) and Long Packets(LPa). For both packet structures, the Data Identifier (DI) is always the first bit of the packet.

5.3.2.8.1 General Packet Structure

Short Packets are four bytes in length including 1 byte DI, 2 bytes data or command and 1 byte Error Correction Code(ECC). The ECC byte is used to check if the first 3 bytes in Packet Header (DI and data) is correct or not. And the ECC byte allows single-bit error to be corrected and 2- bit errors to be detected. The packet format for Short Packets are illustrated as the following.

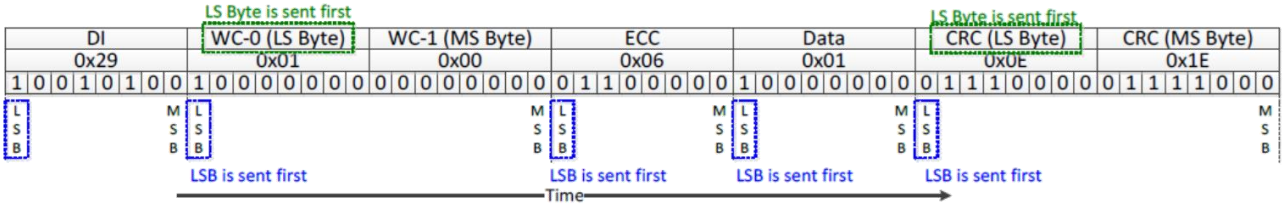


As to Long Packets, they shall consist of three elements: 4 bytes Packet Header, Data Payload with a variable number of bytes and 2 bytes Packet Footer. The Packet Header includes 1 byte DI, 2 bytes Word Count(WC) and 1 byte ECC. The Word Count in Packet Header will decide the number of total bytes of the Data Payload. The Packet Footer has 2 bytes Checksum used to check if the Payload Data is correct or not. The packet format for Long Packets are illustrated as the following.



5.3.2.8.2 Bit Order and Byte Order for Packets

The bit order for packets is the Least Signification Bit sent first and the Most Significant Bit sent last. And for the byte order for packets is the Least Signification Byte sent first and the Most Significant Byte sent last.



5.3.2.8.3 Common Packet Elements

There are several common elements for Long and Short Packets such as DI byte and ECC byte.

The DI byte consists of 2-bit Virtual Channel identifier (VC = DI [7:6]) and 6-bit Data Type field (DT = DI [5:0]). The DI structure is as the following

Data Identifier(DI)							
Virtual Channel(VC)		Data Type(DT)					
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

Virtual Channel is used to assign which peripherals for packets transmission. Data Type specifies if the packet is a Long or Short Packet and the packet format. The Data Type are defined as the table below

Data Type(hex)	Data Type(binary)	Description	Packet Size
0x02	00 0010	Acknowledge and Error Report	Short
0x11	01 0001	Generic Short READ Response, 1 byte returned	Short
0x12	01 0010	Generic Short READ Response, 2 bytes returned	Short
0x1A	01 1010	Generic Long READ Response	Long
0x1C	01 1100	DCS Long READ Response	Long
0x21	10 0001	DCS Short READ Response, 1 byte returned	Short
0x22	10 0010	DCS Short READ Response, 2 bytes returned	Short

Data Types for Processor-Sourced Packets

Data Type(hex)	Data Type(binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x07	00 0111	Compression Mode Command	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short

0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write	Long
0x0A	00 1010	Picture Parameter Set	Long
0x0B	00 1011	Compressed Pixel Stream	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

As to ECC, the host processor shall always calculate and transmit an ECC byte to identify the error for the Packet Header. The bits of ECC are defined as the rule below. The symbol '^' means XOR function. P7 and P6 are set to 0 because Error Correction Code is based on 64-bit value but this ECC implementation is only used for 24-bit value.

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

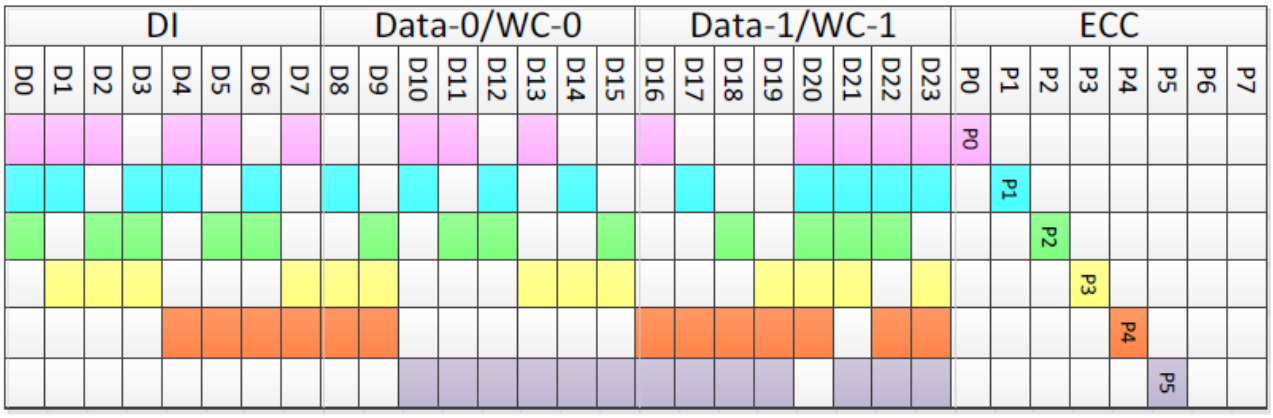
P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

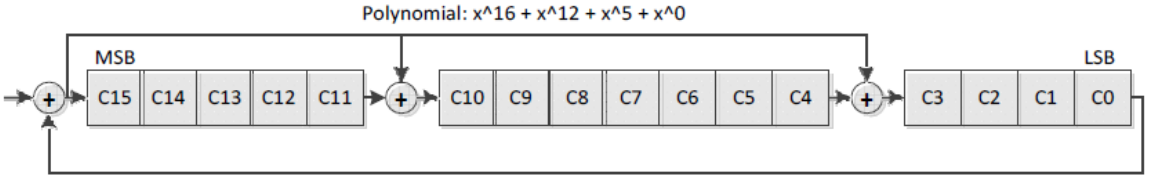
P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23



5.3.2.8.4 Packet Footer for Long Packets

There are two packet structures are defined for communication: Short Packets (SPa) and Long Packets (LPa). For both packet structures, the Data Identifier (DI) is always the first bit of the packet.

The Packet Footer for Long Packets is a checksum value which is calculated from the Data Payload in the Long Packet. The checksum is using a 16-bit Cyclic Redundancy Check (CRC) with a generator polynomial of x^16 + x^12 + x^5 + x^0. The Receiver will calculate checksum value from received Data Payload and compare this CRC value with the Packet Footer sent by transmitter. If calculated CRC values equal to Packet Footer, the received Data Payload are correct. The CRC implementation is presented as the following.



5.3.2.8.5 Packet Pixel Stream Format

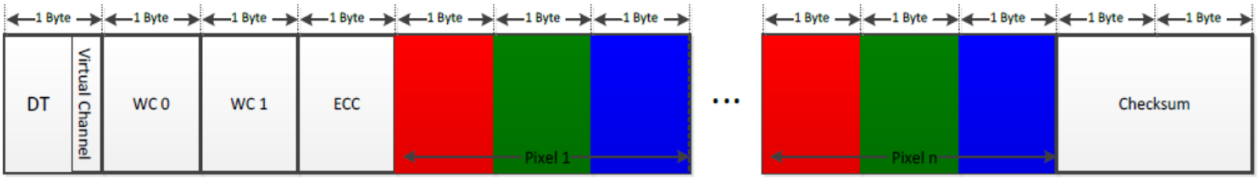
There are 4 packet pixel stream format: 16-bit RGB 5-6-5, 18-bit RGB 6-6-6, loosely packed 18- bit RGB 6-6-6 and 24-bit RGB 8-8-8. The Data Type for these pixel stream format are shown as the table below.

Data Type(hex)	Data Type(binary)	Description	Packet Size
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

Note: 0.39" Micro OLED only support 24-bit RGB pixel stream format

5.3.2.8.6 24-bit RGB Format, Data Type = 0x3E

The data of 24-bit RGB pixel format comprise of eight bits red, eight bits green and eight bits blue. The pixel stream format is shown as the figure below.



5.3.2.9 Peripheral-to-Processor LP Transmissions

All systems require bi-directional capability for returning READ data, acknowledge or error information to the Host Processor. It shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use Low Power mode of Transmission.

Packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction. There are four basic types for peripheral-to-processor transactions: Acknowledge, Acknowledge and Error Report, Response to Read Request, Tearing Effect (TE)

Acknowledge and Error Report is a Short Packet sent if any errors were detected in preceding transmissions from the Host Processor. Once the Errors are reported, the accumulated errors in the error register are cleared.

An error report is a short packet comprised of two bytes following the DI byte and with an ECC byte following the Error Report bytes. Detection and reporting of each error types is signified by setting the corresponding bit to “1”. The bit assignment for all error reporting is shown as the table below.

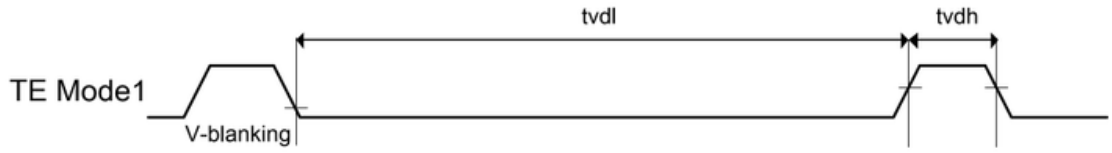
Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, singl-bit(detected and corrected)
9	ECC Error, multi-bit(detected, not corrected)
10	Payload Checksum Error
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

5.4 Tearing Effect Output

The tearing effect (TE) output signal used to be a synchronization signal for command mode display application. A command mode display has its own timing control and memory frame buffer. To avoid tearing effect, it is needed to synchronize timing between host and panel.

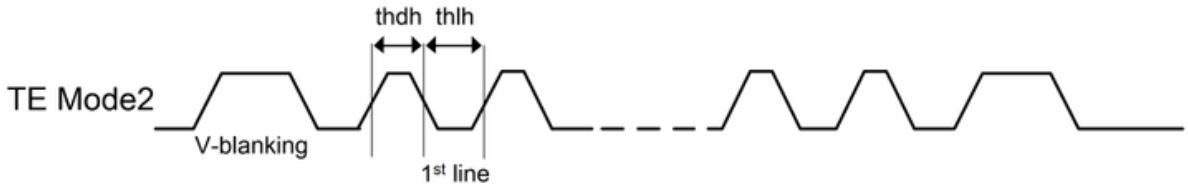
There are three kinds of TE mode supported from display module. These TE output signals can be enable, disable and select by DCS command 35h, 34h and 44h. In below shows the different TE output mode:

TE Mode1: The tearing effect output signal consists of V-Blanking only.

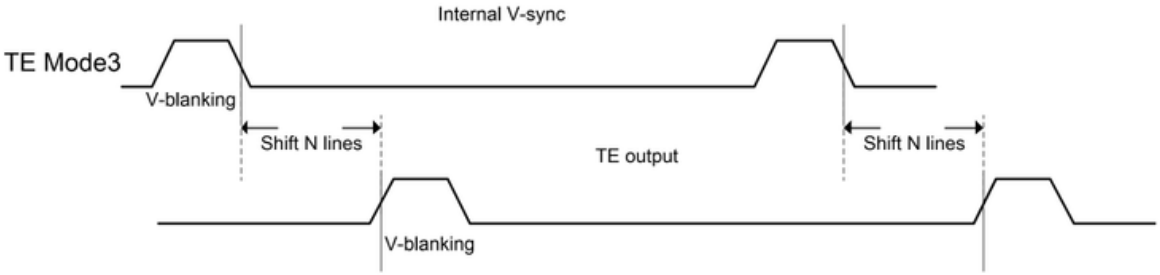


tvdh = display data is not updated the data from memory frame buffer.
tvdl = display data is updated the data from memory frame buffer.

TE Mode2: The tearing effect output signal consists of V-Blanking and H-Blanking.



tvdh = display data is not updated the data from memory frame buffer.
tvdl = display data is updated the data from memory frame buffer.



N = the N-th line after V-blanking, which is set by 44h command.
Mode selection for TE output

TEON (35h), TEOFF (34h)	TEON (35h]), M(bit0)	STESL (44h), N[15:0]	TE Output
TEOFF	X	X	TE off (output low)
TEON	M =0	N[15:0] = 0	TE mode1
TEON	M =1	N[15:0] = 0	TE mode2
TEON	M =0	N[15:0] ≠ 0	TE mode3

6. Electrical Characteristics

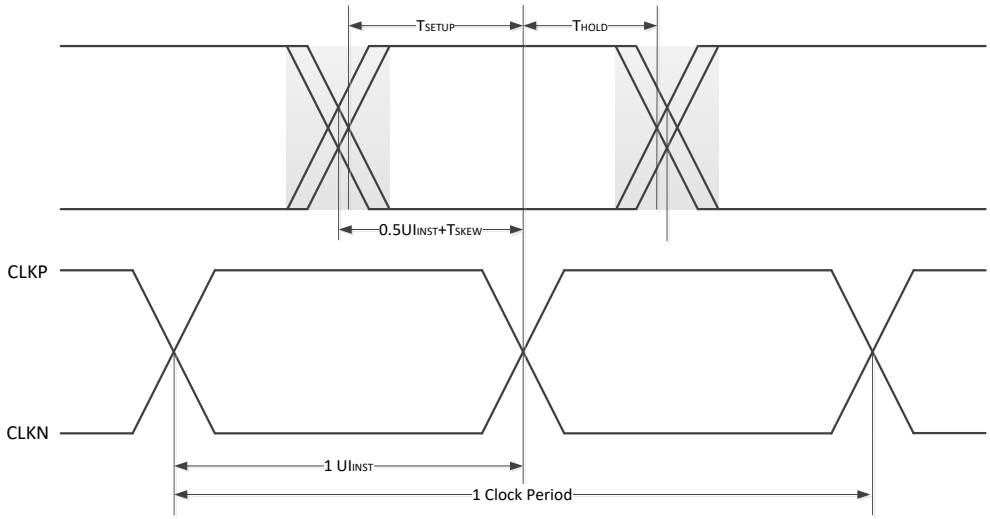
6.1 DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power & Operation Voltage/Current For FPC Module						
AVDD Input Level	AVDD Voltage	-	5.7	6	6.1	V
	AVDD Input Current	-		25	-	mA
AVEE Input Level	AVEE Voltage	-	-5.7	-6	-6.1	V
	AVEE Input Current	-		20	-	mA
VDDI Input Level	VDDI Voltage	-	1.65	1.8	1.95	V
	VDDI Input Current	-		40	-	mA
MIPI I/O Power Supply	MVDD	-	-	1.2	-	V

6.2 AC Characteristics

6.2.1 MIPI High Speed Mode Characteristics

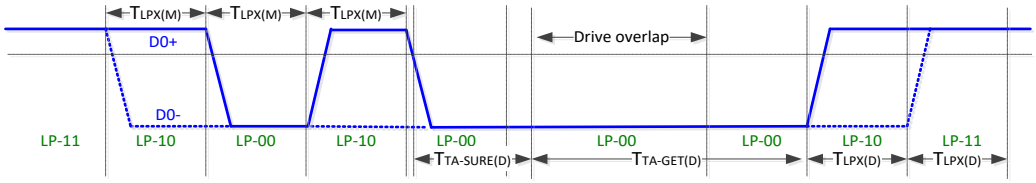
Parameter	Symbol	Min	Typ.	Max	Unit
UI instantaneous	UIINST	1	-	3	ns
T Data to Clock Skew	TSKEW	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	TSETUP	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	THOLD	0.15	-	-	UIHS



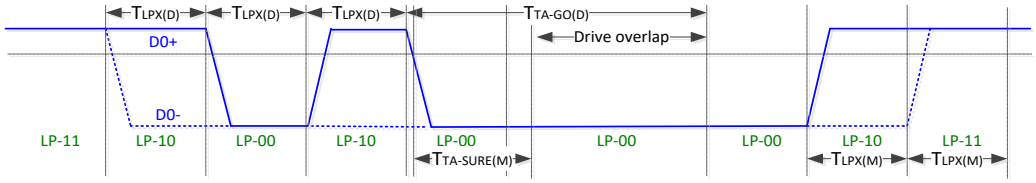
6.2.2 MIPI Low Power Mode Characteristics

Parameter	Description	Min	Typ.	Max	Unit
$T_{LPX(M)}$	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state(LP-00) during a Link Turnaround	T_{LPX}	-	$2*T_{LPX}$	
T_{TA-GET}	Time that the new transmitter drives the Bridge state(LP-00) after accepting control during a Link Turnaround	$5*T_{LPX}$			
T_{TA-GO}	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround	$4*T_{LPX}$			

- Bus Turnaround from MPU to display module



- Bus Turnaround from display module to MPU



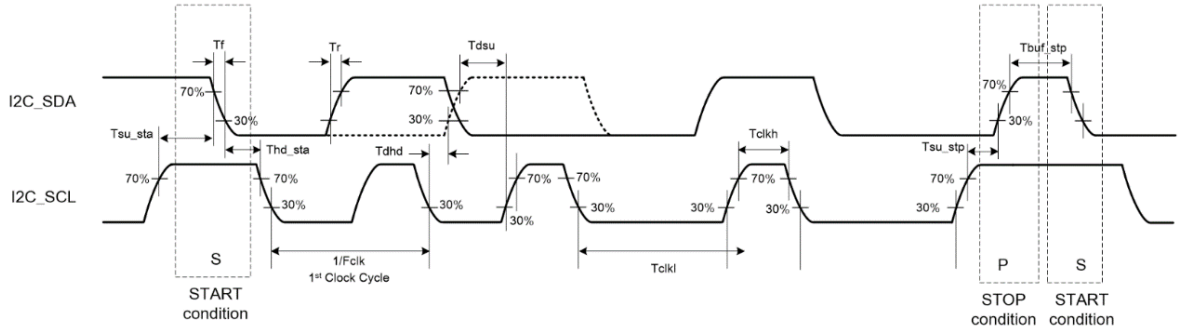
6.2.3 MIPI Video Timing Specification.

1920×1080@60Hz					
H	Hsync	44	V	Vsync	4
	HBP	148		VBP	8
	Hactive	1920		Vactive	1080
	HFP	88		VFP	8
Recommended configuration of MIPI					
D-PHY V1.2 DSI 1.01	CLK Mode: Discontinue Mode				
	MIPI Lane: 4 Lanes@60Hz.				
	Video Mode: Burst Mode				
	HS Speed: 300Mbps ~ 1.0Gbps per Lane				
	LP Speed: 10Mbps（max）				
	General Packet Structure：DCS Mode .Data Type of Packet：0x39 or 0x05 or 0x15				

※This parameter is a typical example illustrating the display timing. Huaxin cannot assume responsibility for any problems arising out of the use of the circuit.

6.2.4 I2C Interface Timing

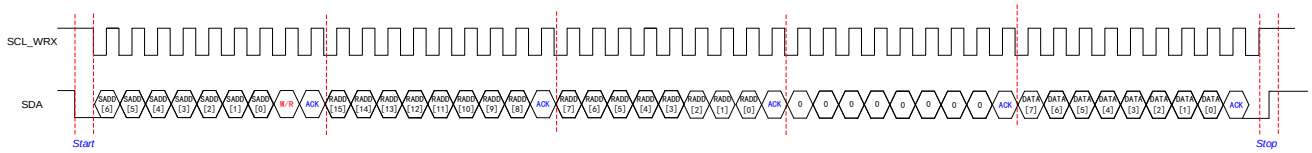
Parameter	Symbol	Min.	Typ.	Max.	Unit
I2C Clock Frequency	Fclk	-	-	400	kHz
I2C Clock Low	Tclkl	1300	-	-	ns
I2C Clock High	Tclkh	600	-	-	ns
I2C Data Rising Time	Tdr	-	-	300	ns
I2C Data Falling Time	Tdf	-	-	300	ns
I2C Data Setup Time	Tdsu	100	-	-	ns
I2C Data Hold Time	Tdhd	-	-	TBD	ns
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns
I2C Bus Free Time (Stop Condition)	Tbuf_stp	1300	-	-	ns



Notes:

No.	ITEM	Description	Note
1	Slave address	0x4C	
2	Pull-up resistor	4.7KΩ@100Kbps	
3	Read bit	Setting “1” for write	
4	Write bit	Setting “0” for write	
5	Start condition	SDA is setting from “1” to “0” when SCL is “1”	
6	Stop condition	SDA is setting from “0” to “1” when SCL is “1”	

6.2.5 I2C Interface Waveform



SADD[6:0]—Slave address.
W—Write bit. R—Read bit. W=0. R=1.
ACK—Acknowledge bit. ACK=0.
RADD[15:0]—Register address. RADD[7:0] is for shifting.

Code Example:

MIPI format: *regw 0x51 0xFF 0x01*

IIC format: *regw 0x51 0x00 0x00 0xFF*

regw 0x51 0x01 0x00 0x01

6.3 Power Consumption

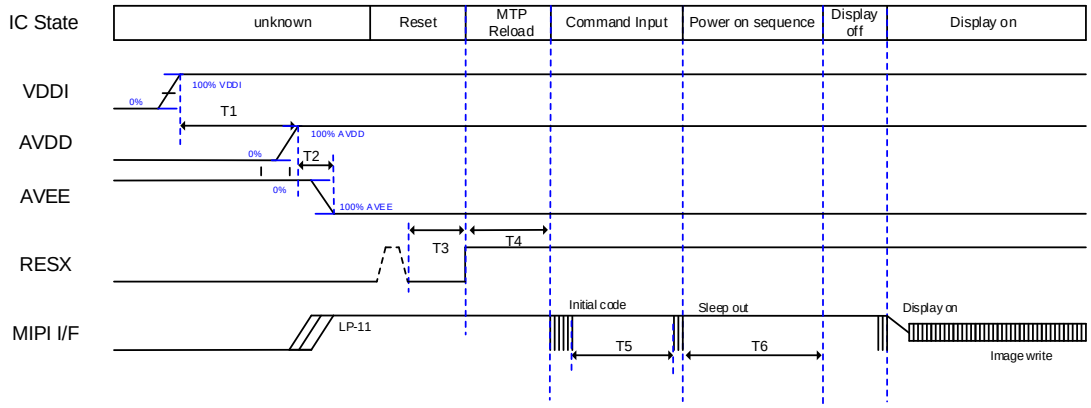
Symbol	Condition	1000cd/m^2	Unit
Total power	- Tpnl = 40 ℃	<350	mW

Note: All white raster display, clock frequency=148.5MHz, frame rate=60Hz. White（L255）.

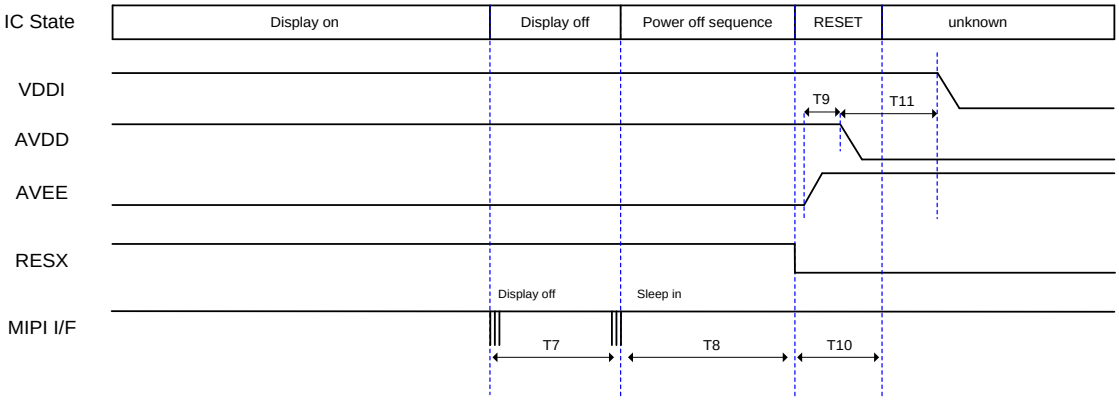
7. Power Supply Sequence

7.1 Power On/Off Sequence

Power on sequence For FPC Module



Power off sequence For FPC Module



Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between AVDD(VIN) and VDDI
T2	0	-	-	ms	Power on time between AVDD and AVEE. AVDD cannot be later than AVEE
T3	1	-	-	ms	Effective hardware reset period
T4	20	-	-	ms	MTP reload time
T5	0	-	-	ms	The time is between initial code finished and sleep-out command
T6	2	-	8	VS	Power on sequence, the period can be modified
T7	1	-	-	VS	Blanking region
T8	-	1	-	VS	Power off sequence, the period can be modified
T9	0	-	-	ms	Power off time between AVEE and AVDD. AVDD cannot be earlier than AVEE
T10	1	-	-	ms	Effective hardware reset period
T11	1	-	-	ms	Power off time between AVDD(VIN) and VDDI

8. Description of Function

8.1 Display Mode

8.1.1 Power Mode

ITEM	Code value
Sleep In	0x10
Sleep Out	0x11
Display On	0x29
Display Off	0x28

8.1.2 Idle Mode

ITEM	Code value
Idle On	0x39(Default value)
Idle Off	0x38

8.1.3 BIST Mode

Register setting：

BIST On/Off Control (C4h)

<table>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address name</td><td colspan="9">Parameter</td></tr>
<tr><td>MIPI</td><td>I2C</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="4">BISTONOFF</td><td rowspan="4">R/W</td><td rowspan="4">C4h</td><td>C400h</td><td>-</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>C401h</td><td>-</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>C402h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>BION1</td></tr>
<tr><td>C403h</td><td>-</td><td>BION2</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to control BIST function (Free Run mode).
BIST function enable step:
1. Enter Sleep-In (10h) mode.
2. Setting PATENICYC [1:0] and BISTPATEN[11:0] to control the display cycle time and pattern.
3. Setting BION1=”1” and BION2=”1”, the driver IC will start to run the BIST function.
BIST function disable step:
1. Setting BION1=”0” and BION2=”0”,the driver IC will return to normal function.
2. Sending MIPI video data and enter Sleep-Out (11h) mode for normal display.</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td colspan="2">Default Value</td></tr><tr><td rowspan="4">Power On Sequence</td><td>C400h</td><td>AAh</td></tr><tr><td>C401h</td><td>55h</td></tr><tr><td>C402h</td><td>00h</td></tr><tr><td>C403h</td><td>00h</td></tr></table></td></tr>
</table>

BIST CTRL (C5h)

Instruction	R/W	Address name		Parameter								
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BISTSET	R/W	C5h	C500h	-	0	0	PATENICYC[1:0]		BISTPATEN[11:8]			
			C501h	-	BISTPATEN[7:0]							
			C502h	-	GRAY_LEVEL[7:0]							

Description

This command is used to set the display pattern in BIST function.

PATENICYC [1:0] : Cycle time between each display pattern.

PATENICYC[1:0]	Pattern cycle time
0h	256 Frame
1h	512 Frame
2h	1024 Frame
3h	2048 Frame

BISTPATEN [11:0] : Select the display pattern in BIST function.

BISTPATEN[9:0]	Description
BISTPATEN[0]	Red pattern.
BISTPATEN[1]	Green pattern.
BISTPATEN[2]	Blue pattern.
BISTPATEN[3]	Black pattern.
BISTPATEN[4]	Gray Level pattern. (Set by BIST_GRAY_LEVEL[7:0])
BISTPATEN[5]	Vertical Gradation pattern.
BISTPATEN[6]	Horizontal Gradation pattern.
BISTPATEN[7]	Color Bar pattern.
BISTPATEN[8]	Crosstalk with boundary pattern.
BISTPATEN[9]	Source CP Pattern
BISTPATEN[10]	Gamma CP Pattern
BISTPATEN[11]	Reserved

Note1: the patterns which the bit number of BISTPATEN[9:0] is set to "1" will display and change automatically.

Note2: When BISTPATEN [11:0] =12'h000, display pattern will be black pattern.

GRAY_LEVEL [7:0] : Set the gray level when BISTPATEN [4]="1" in BIST function.

GRAY_LEVEL[7:0]	Description
0h	Gray Level : 00h
1h	Gray Level : 01h
2h	Gray Level : 02h
:	:
FDh	Gray Level : FDh
FEh	Gray Level : FEh
FFh	Gray Level : FFh

Restriction: -

Default

Status	Default Value	
Power On Sequence	C500h	01h
	C501h	FFh
	C502h	FFh

8.1.4 Command Enable Mode

F000H	MAUCCTR											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
			F000h	-	1	0	1	0	1	0	1	0

MAUCCTR	W	F0h	F001h	-	-	-	-	EN_CMD2	PAGE[3:0]

Description

This command is used to enable the access of CMD2 page.

Bit	Symbol	Description	Comment
D4	EN_CMD2	Enable access of CMD2 page	1= enable 0= disable
D[3:0]	PAGE[3:0]	CMD2 Page selection	0=CMD2 Page0 1=CMD2 Page1 2=CMD2 Page2 3=CMD2 Page3 4=CMD2 Page4 Others=Reserved

Restriction

-

Default

Status	Default Value	
Power On Sequence	F000h	AAh
	F001h	00h

8.2 Brightness Control (BC) Functions

This function adjusts the gamma parameter according to the register 51h and 53h setting to adjust the luminance.

BCCTR3 (C2h):

C2H	WRCTRLD											
Instruction	R/W	Address		Parameter								
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BCCTR3	R/W	C2	C200h	-	EM_WD_0[7:0]							
			C201h		EM_WD_1[7:0]							
			C202h		EM_WD_2[7:0]							

Description

EM-WD-x [7:0]: Duty ratio of Emission for DBV_P00~P03.

EM_WD_0[7:0] EM_WD_1[7:0] EM_WD_2[7:0]	Duty ratio of Emission for DBV_P00~P03
0h	1/256
1h	2/256
.	.
FEh	255/256
FFh	256/256

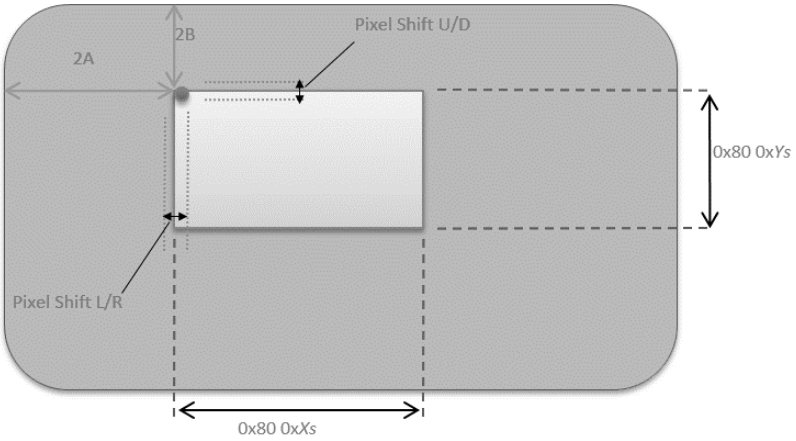
Restriction

Default

Status	Default Value	
Power On Sequence	C200h	00h
	C201h	00h
	C202h	00h

8.3 Display Active-Area (AA) Control

ITEM	Description	Code value
Resolution	X-direction: Support 8N, N=40~240 Y-direction: support 8M, M=30~135	CMD1：0x80(NC[7:0] NL[7:0])
Active-Area(AA) control	Display start pointer	Xs：CMD1：0x2A Ys：CMD1：0x2B
	Pixel shift：±12pixel/step=4pixel	CMD2 Page0：0xB4



8.3.1 Resolution (80h CMD1)

8000H	RESCTRL1											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-8	D7	D6	D5	D4	D3	D2	D1	D0
RESCTRL1	R/W	80h	8000h	-	-	-	-	-	-	-	-	OSC_FREQ_SEL
			8001h	-	NC[7:0]							
			8002h	-	NL[7:0]							

Description

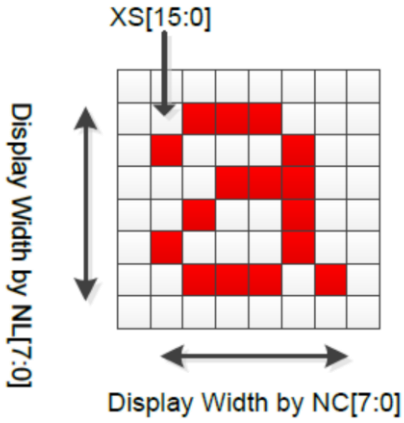
This command is used to set panel type and display resolution.

Bit	Symbol	Description	Comment
D0	OSC_FREQ_SEL	OSC frequency selection	0= 80MHz 1= 60MHz
D[7:0]	NC[7:0]	X-axis resolution for display image size	X-axis resolution for display image size= NC[7:0]*8
D[7:0]	NL[7:0]	Y-axis resolution for display image size	Y-axis resolution for display image size= NL[7:0]*8

Restriction	Resolution switch is only valid in *SLPIN* mode.
Default	

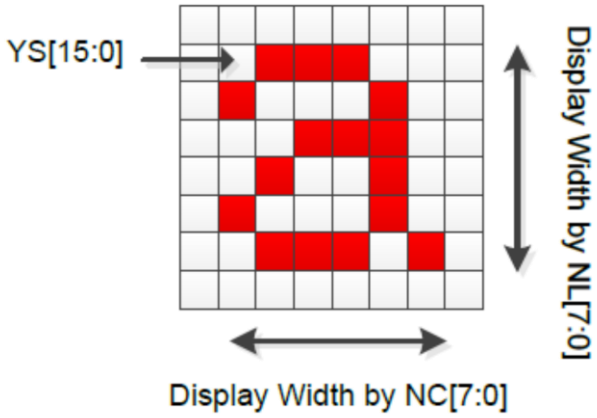
Status	Default Value	
Power On Sequence	8000h	01h
	8001h	F0h
	8002h	87h

8.3.2 Active-Area (AA) control Column Address Set (2Ah CMD1)

2A00H	WRCTRLD											
Instruction	R/W	Address		Parameter								
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RESCTRL 1	W	2Ah	2A00h	-	XS[15:8]							
			2A01h		XS[7:0]							
Description	This command indicates display start position of display module in columns. XS[15:0]: Display line start position  											
Restriction	1. XS= 0 + 4N, N=integer 2. Display content cane be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, and PIXEL_SHIFT_Y_COUNT. The constraint is that display content can't exceed display area. XS should follow the rule as below: PIXEL_SHIFT_X_DIR=0(Left) Parameter range= 0 ≤ XS[15:0] + NC[7:0]*8 - PIXEL_SHIFT_X_COUNT*4 ≤ 1944 (798h) PIXEL_SHIFT_X_DIR=1(Right) Parameter range= 0 ≤ XS[15:0] + NC[7:0]*8 + PIXEL_SHIFT_X_COUNT*4 ≤ 1944 (798h)											
Default												

Status	Default Value	
Power On Sequence	2A00h	00h
	2A01h	00h

8.3.3 Active-Area (AA) control Row Address Set (2Bh CMD1)

2B00H	WRCTRLD										
Instruction	R/W	Address		Parameter							
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RESCTRL1	W	2Bh	2B00h	-	YS[15:8]							
			2B01h		YS[7:0]							
Description	This command indicates display start position of display module in rows. YS[15:0]: Display line start position 										
Restriction	3. YS= 0 + 4N, N=integer 4. Display content cane be adjusted by XS, YS, PIXEL_SHIFT_X_COUNT, and PIXEL_SHIFT_Y_COUNT. The constraint is that display content can't exceed display area. YS should follow the rule as below: PIXEL_SHIFT_Y_DIR=0(Up) Parameter range= 0 ≤ YS[15:0] + NL[7:0]*8 - PIXEL_SHIFT_Y_COUNT*4 ≤ 1104 (450h) PIXEL_SHIFT_Y_DIR=1(Down) Parameter range= 0 ≤ YS[15:0] + NL[7:0]*8 + PIXEL_SHIFT_Y_COUNT*4 ≤ 1104 (450h)										
Default	Status	Default Value									
	Power On Sequence	2B00h	00h								
		2B01h	00h								

8.3.4 Active-Area (AA) control Pixel shift s Set (B4h CMD1)

Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
PXLSHIFT CTR	R/W	B4h	B400h	-	PIXEL_SHIFT_X_DIR	-		PIXEL_SHIFT_X_COUNT[4:0]				
			B401h	-	PIXEL_SHIFT_Y_DIR	-		PIXEL_SHIFT_Y_COUNT[4:0]				

Description

PIXEL_SHIFT_X_DIR: Pixel shift direction of X-axis

PIXEL_SHIFT_X_DIR	Pixel Shift Direction of X-axis
00h	Left
01h	Right

PIXEL_SHIFT_X_COUNT[4:0]: Pixel shift of X-axis

PIXEL_SHIFT_X_COUNT[4:0]	Pixel Shift of X-axis
00h	0-pixels
01h	4-pixels
02h	8-pixels
03h	12-pixels

PIXEL_SHIFT_Y_DIR: Pixel shift direction of Y-axis

PIXEL_SHIFT_Y_DIR	Pixel Shift Direction of Y-axis
00h	Up
01h	Down

PIXEL_SHIFT_Y_COUNT[4:0]: Pixel shift of Y-axis

PIXEL_SHIFT_Y_COUNT[4:0]	Pixel Shift of Y-axis
00h	0-pixels
01h	4-pixels
02h	8-pixels
03h	12-pixels

8.4 Scan direction selection

mipi.write 0x39 0x36 0x00(Default)	Original
mipi.write 0x39 0x36 0x01 mipi.write 0x39 0xF0 0xAA 0x13 mipi.write 0x39 0xC1 0x00 0x12 0x53 0x64 0x31 0x42 0x56 mipi.write 0x39 0xF0 0xAA 0x14 mipi.write 0x39 0xB0 0x0E 0x00 0xEC mipi.write 0x39 0xB6 0x12 0x53 0x64 0x31 0x42 0x56	Only Y-direction mirror
mipi.write 0x39 0x36 0x02	Only X-direction mirror
mipi.write 0x39 0x36 0x03 mipi.write 0x39 0xF0 0xAA 0x13 mipi.write 0x39 0xC1 0x00 0x12 0x53 0x64 0x31 0x42 0x56 mipi.write 0x39 0xF0 0xAA 0x14 mipi.write 0x39 0xB0 0x0E 0x00 0xEC mipi.write 0x39 0xB6 0x12 0x53 0x64 0x31 0x42 0x56	X+Y-direction mirror

8.5 Read module display status

8.5.1 Read Display Power Mode (0Ah CMD1)

0A00H	**WRCTRLD**											
Instruction	R/W	Address		Parameter								
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	R	0Ah	0A00h	-	D7	D6	-	D4	D3	D2	-	-

<table>
<tr><td>Description</td><td>This command indicates the status of display driver’s power and operation mode:
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D7</td><td>BSTON</td><td>Boost Status</td><td>1=Boost On
0=Boost Off</td></tr>
<tr><td>D6</td><td>IDMON</td><td>Idle Mode On/Off</td><td>1=Idle Mode On
0=Idle mode Off</td></tr>
<tr><td>D4</td><td>SLPON</td><td>Sleep In/Out</td><td>1=Sleep Out
0=Sleep In</td></tr>
<tr><td>D3</td><td>NOR</td><td>Display Normal Mode On/Off</td><td>1= Display Normal On
0= Display Normal Off</td></tr>
<tr><td>D2</td><td>DISPON</td><td>Display On/Off</td><td>1=Display On
0=Display Off</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td>Power On Sequence</td><td>0A00h</td><td>08h</td></tr>
</table></td></tr>
</table>

8.5.2 MIPI Error Report (68h CMD1)

<table>
<tr><th>2B00H</th><th colspan="11">WRCTRLD</th></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address</td><td colspan="9">Parameter</td></tr>
<tr><td>MIPI</td><td>I2C</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="2">MERR</td><td rowspan="2">R</td><td rowspan="2">68h</td><td>6800h</td><td>-</td><td colspan="8">ERPA[15:8]</td></tr>
<tr><td>6801h</td><td></td><td colspan="8">ERPA[7:0]</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to read DSI errors of MIPI port A
<table>
<tr><th>Symbol</th><th>Description</th></tr>
<tr><td>ERPA[15]</td><td>DSI Protocol Violation</td></tr>
<tr><td>ERPA[14]</td><td>Reserved</td></tr>
<tr><td>ERPA[13]</td><td>Invalid Transmission Length</td></tr>
<tr><td>ERPA[12]</td><td>DSI VC ID Invalid</td></tr>
<tr><td>ERPA[11]</td><td>DSI Data Type Not Recognized</td></tr>
<tr><td>ERPA[10]</td><td>Payload Checksum Error(Long packet only)</td></tr>
<tr><td>ERPA[9]</td><td>ECC Error, multi-bit (detected, not corrected)</td></tr>
<tr><td>ERPA[8]</td><td>ECC Error, single-bit (detected, not corrected)</td></tr>
<tr><td>ERPA[7]</td><td>Contention Detected</td></tr>
<tr><td>ERPA[6]</td><td>False Control Error</td></tr>
<tr><td>ERPA[5]</td><td>Peripheral Timeout Error</td></tr>
<tr><td>ERPA[4]</td><td>Low-Power Transmit Sync Error</td></tr>
<tr><td>ERPA[3]</td><td>Escape Mode Entry Command Error</td></tr>
<tr><td>ERPA[2]</td><td>EoT Sync Error</td></tr>
</table></td></tr>
</table>

	ERPA[1]	SoT Sync Error
	ERPA[0]	SoT Error
Restriction		
Default	Status	Default Value
	Power On Sequence	6800h: 00h
		6801h: 00h

9. Optical Characteristics

9.1 Optical Characteristics

Item			Specification
White Brightness (255 Level)	L		1000 ±20% cd/m^2
White Uniformity 9 Point	White (255 Level)		>80%
View Angle (White)	Lum.Decay (50%)		-15 °~15 °
	Color Shift(Δu'v'<0.025)		-10 °~10 °
Contrast	CR		>5000:1
Color Coordinate	Red	CIE-x	0.648 ±0.050
		CIE-y	0.347 ±0.050
	Green	CIE-x	0.226 ±0.050
		CIE-y	0.689 ±0.050
	Blue	CIE-x	0.145 ±0.050
		CIE-y	0.065 ±0.050
	White	CIE-x	0.31 ±0.05
		CIE-y	0.33 ±0.05
Color Gamut(NTSC)			>60%
Color Temperature			>5000K

Notes:

1. The brightness of the product will be measured after 5 minutes of stabilization for the white screen at room temperature.

2. The formula of the brightness uniformity at 9 points of the white screen is Uniformity=1-(Max. -Min.)/ (Ave.), and the Max., Min. and Ave. represent the maximum, minimum and average of the brightness of 9 points, respectively.

9.2 Measurement System /Measurement Method

The luminance and chromaticity are measured in Measurement System A shown below.

Measurement temperature: Tpnl = 40 ℃

Measurement point: One point on the screen center

All white display: All RGB signal data is set to High.

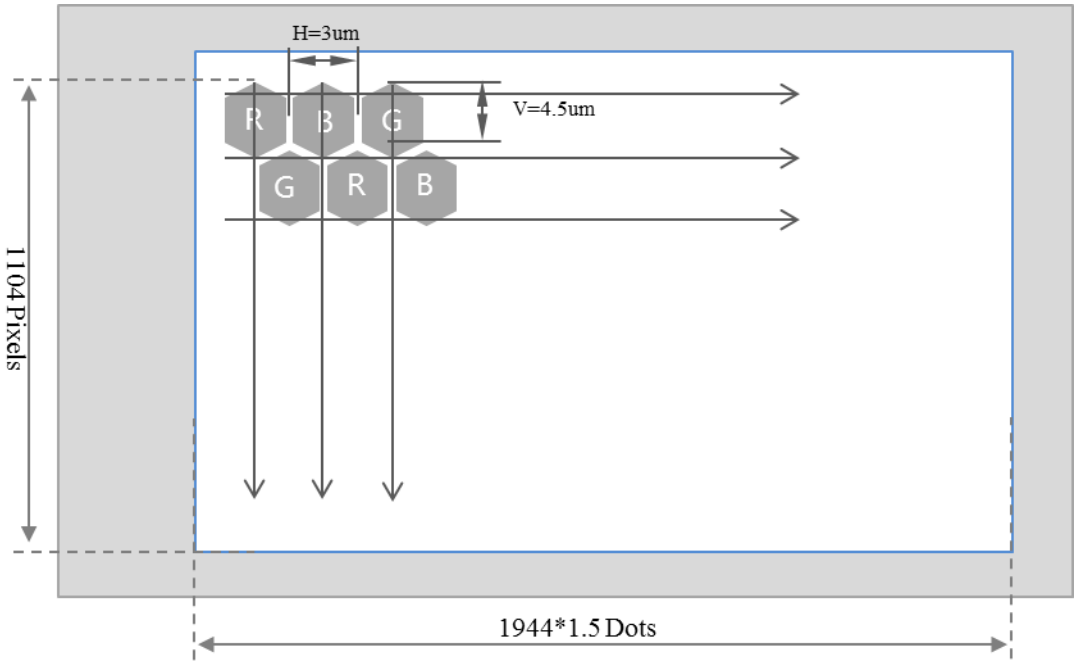
All black display: All RGB signal data is set to Low.

Luminance and chromaticity: Measure the luminance and chromaticity in all white display in Measurement System A.

Contrast: Measure the luminance in all white display (@ : 1000cd/m^2) and all black display in Measurement System A, and substitute them into the formula below.

Contrast = Luminance in all white display/Luminance in all black display

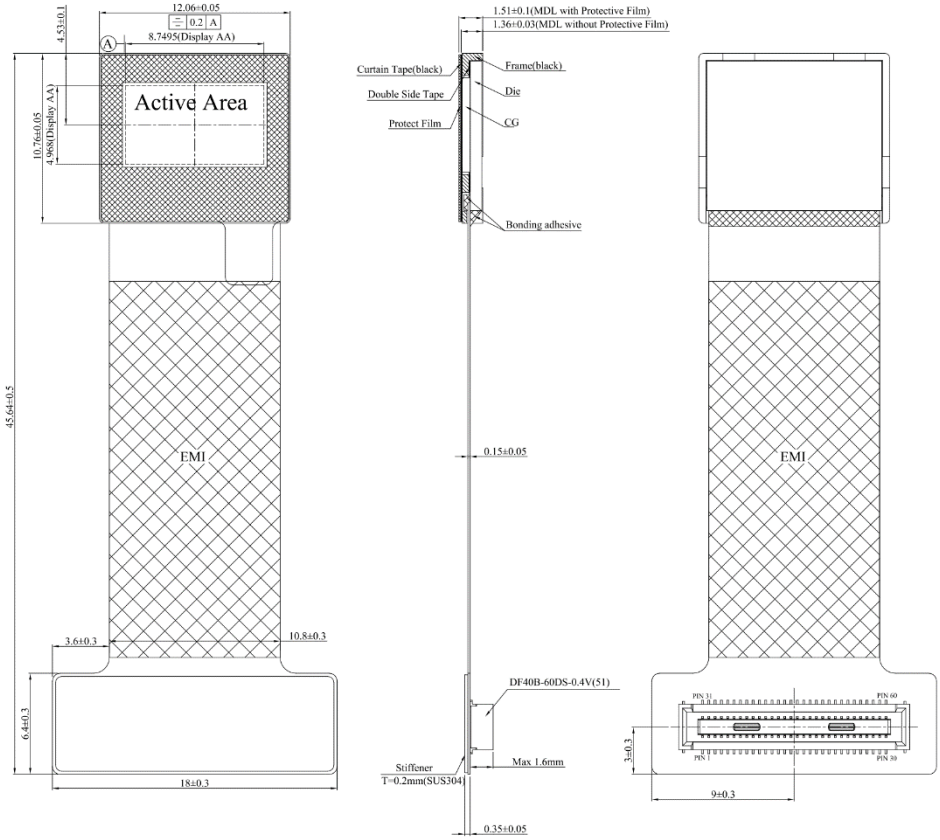
10. Pixel Alignment



※Including orbit margin

11. Package Outline

11.1 FPC Module(Unit：mm)



Note:

1. The connector models of the FPC module is DF40B-60DS-0.4V (51), and the corresponding connector model is DF40B-60DP-0.4V (51).

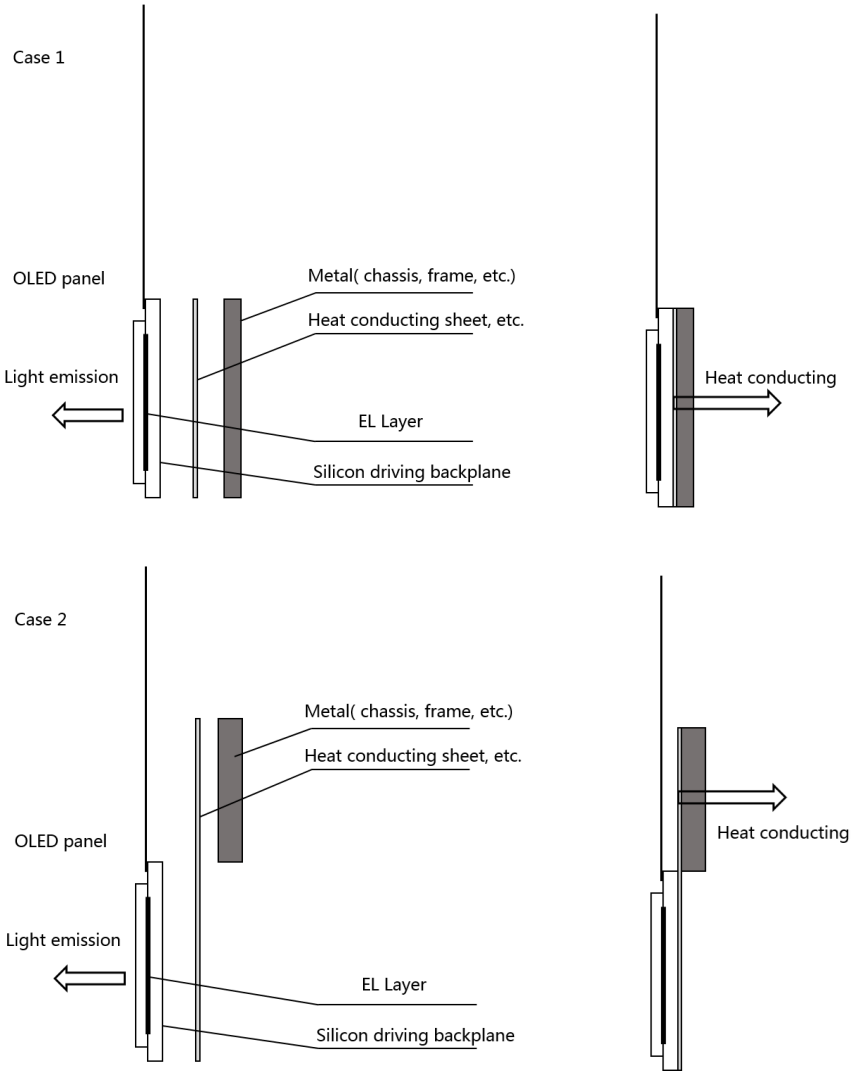
2. The FPC bending Angle ≤180°, FPC bending radius ≥ R2 mm, the distance between bending line and die edge ≥1.5mm.

12. Recommended Items

12.1 Suppression of the Panel Temperature

Temperature of organic EL panel tends to rise due to power consumption (heat generation) by the EL emission layer and the integrated silicon drive circuit. The temperature rise may cause luminance rise at initial state, or luminance drop by over time.

The temperature change in panel can be suppressed by establishing a thermal connection between panel rear surface (silicon substrate surface) and metal (chassis, frame, metal structure, etc.) at panel mount area, and the heat conducting sheet size can be changed, So highly recommend the heat conductive sheet between them as show in below. In order to ensure the normal operation of the screen, heat dissipation must be done to ensure that the screen temperature < 60℃.



13. Notes on Handling

13.1 Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

(1) Use non-chargeable gloves.

(2) Use a wrist strap connecting ground when handling.

(3) Do not touch any electrodes on the panel.

(4) Wear non-chargeable clothes and conductive shoes.

(5) Install grounded conductive mats on the working floor and working table.

(6) Keep the panel away from any charged materials.

13.2 Protection from dust and dirt

(1) Operate in a clean environment.

(2) Do not touch the panel surface. The surface is easily scratched.

When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on

the surface.

(3) Use ionized air to blow dust off the panel surface.

13.3 Others

(1) Not hold FPC (Flexible Printed Circuit) , not twist the FPC, not bend FPC because connection area between the FPC and panel is easily broken by mechanical stress.

(2) The minimum fold radius of the FPC is 1.0 mm, So do not fold the FPC less than 1.0mm radius.

(3) Do not drop the module.

(4) Do not twist or bend the module .

(5) Keep the module away from heat sources.

(6) Not be close the module to water or other solvents.

(7) Do not store or use the module at high temperatures or high humidity circumstance, as the circumstance may affect module specifications.

(8) When disposing of this, regard it as industrial waste and please comply with related regulations.

(9) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications.

(10) Please take appropriate ESD protection measures (ESD：Contact±1KV，Air±2KV).

(11) Packing Reliability Test

Parking Drop：the test should be applied on 1 corner,3edges,6 sides,80cm

Parking VIB：5~300Hz，1.49Grms，Z/X/Y，Per 1hr